Technology Platforms & Challenges for 3D GaN Power Converters Packaging

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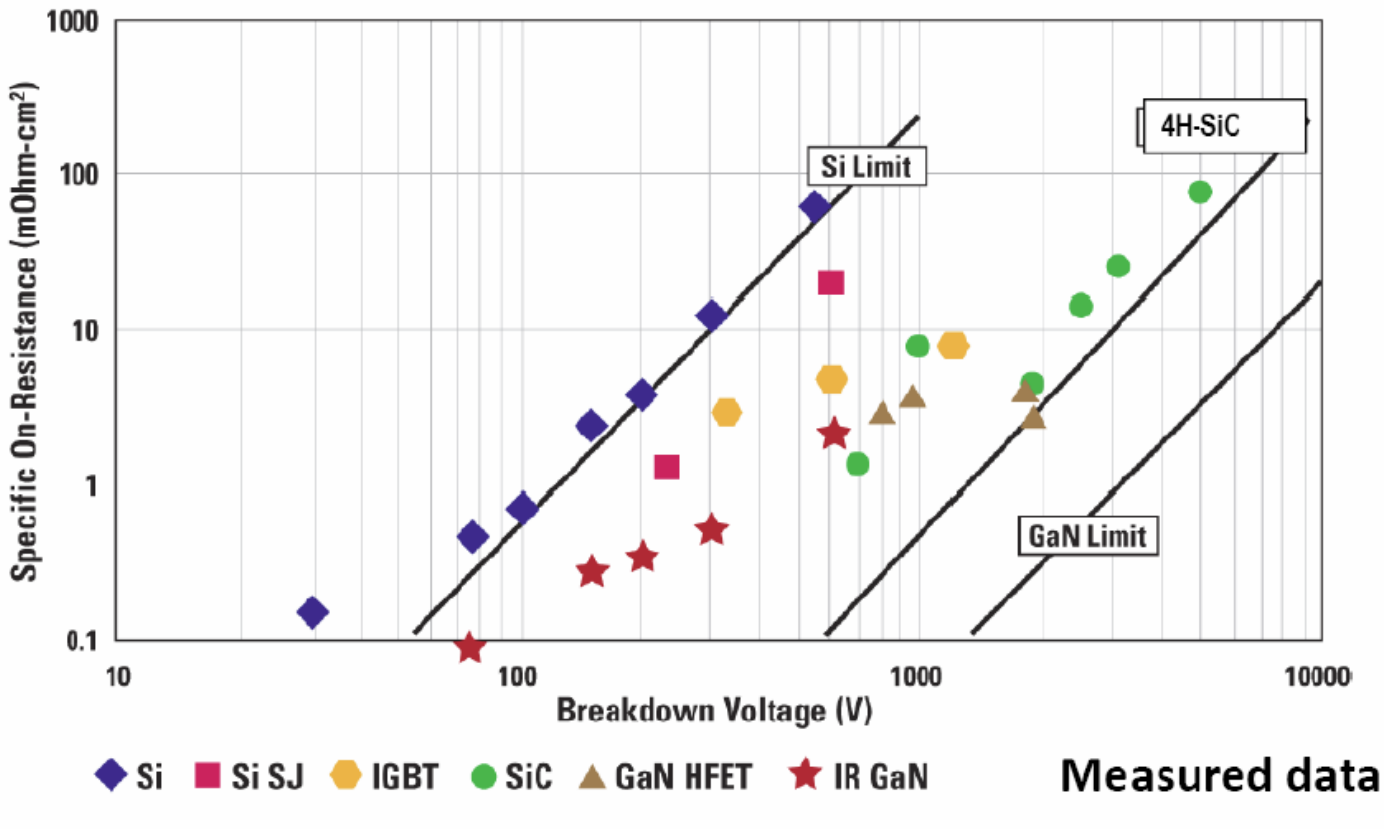
PwrSoC 2014

Acknowledgment:

J.A. Ferreira (TUDelft), J.D van Wyk (UJ), F. Pansier (ex. NXP/TUDelft)

The promise of GaN

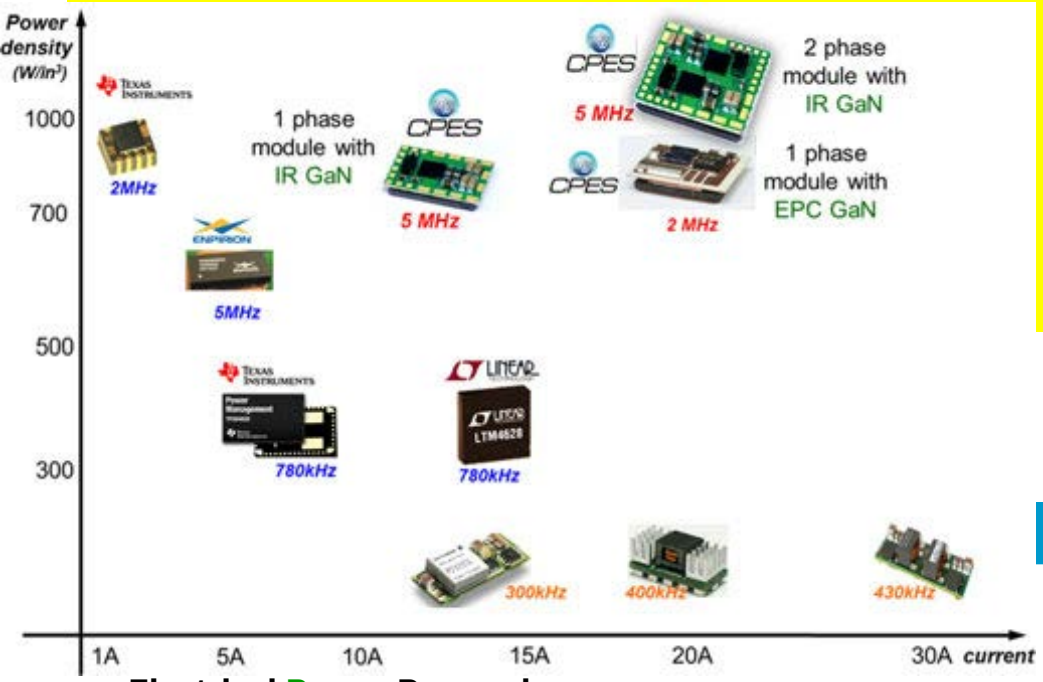


R(on) vs. Blocking Capability for Si, SiC and GaN

N. Ikeda, ISPSD 2008

- Lower losses –> higher efficiency, less thermal management
- Higher switching frequency –> miniaturisation (MHz operation of off-line power supplies)
- Lateral integration –> line voltage power converters on chips
- Higher operating temperature –> more A/mm^2, (high temperature applications?)
- Cost – WBG performance at cost of Si

Panasonic, 2009.

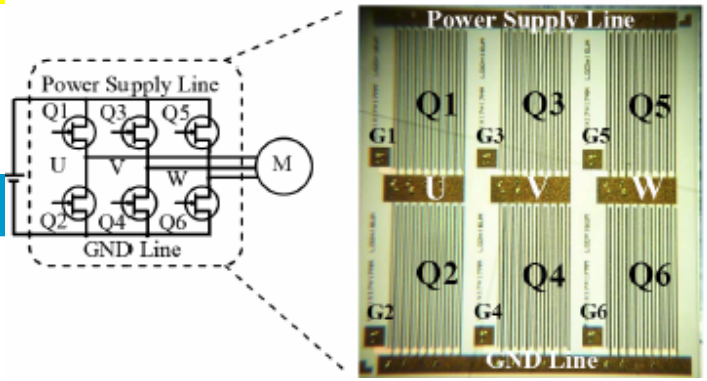


Electrical Power Processing

S. Ji et al. IEEE PELS 2013

Lateral Integration: Panasonic

GaN monolithic inverter IC
- w_G = 25 mm/transistor
- chip size: 2.5 x 2.7 mm



- WBG device: “perfect” switch (or at least an order of magnitude better)
- BUT: Parasitics and thermal management do not scale
- How to fully exploit it?
  - Better (*converter*) packaging and assembly
  - Better circuit design
  - Better thermal management

Content

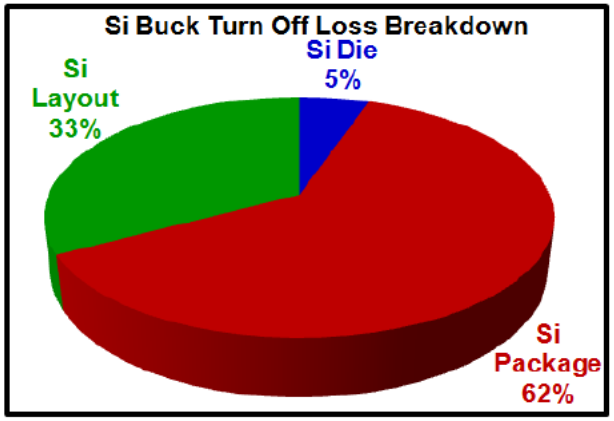
- Parasitics (components, package, layout)
- Thermal management (vs. high frequency switching)
- 3D system integration
- Final remarks

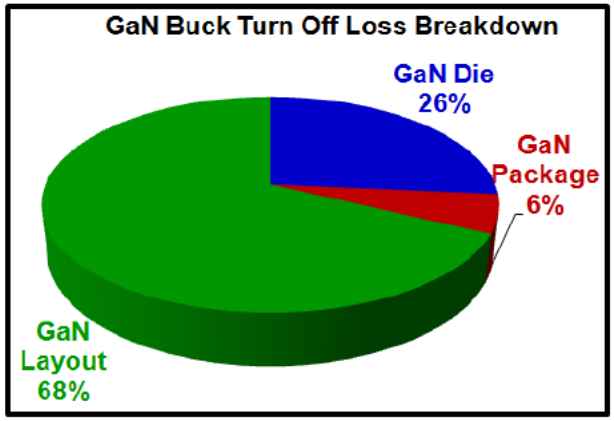
Parasitics

- Limits of hard switching – package and circuit parasitics dominate the circuit behaviour and losses
  - LV devices (<200V), chip-size packages have low package inductance (0.15nH vs 0.7nH of LFPAK) -> loop inductance instead of common source inductance dominates losses

EPC

J. Wurfl, ECPE Seminar on WBG devices 2013



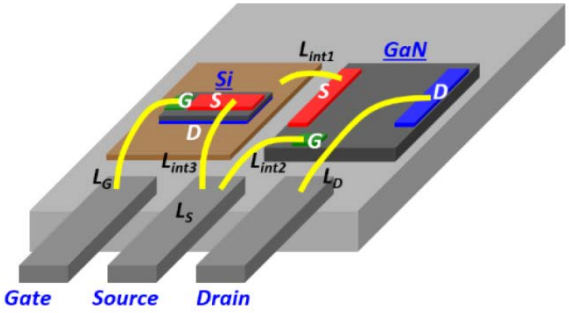


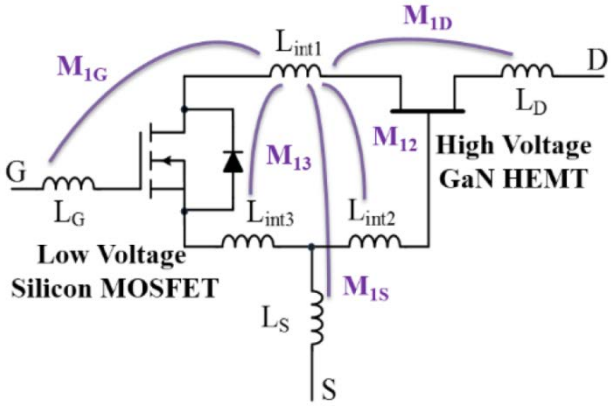
D. Reusch, PhD thesis, Virginia Tech

Turn off loss breakdown of PCB layout, die, and package of
(a) Si benchmark using LFPAK devices , eff 85%@1MHz
(b) GaN design (2nH loop inductance), eff 89% @1MHz

- HV (600V) devices, cascode configuration
  - Through-hole (TO-220) – critical package inductances almost double the switching loss

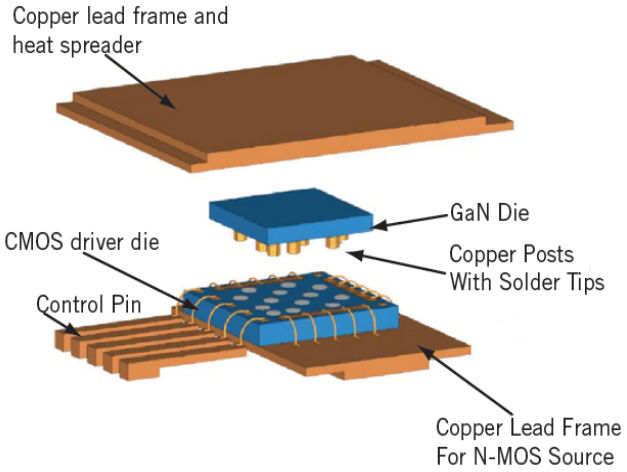
Transphorm





  - Direct mounting of GaN die on the Si die

GaN systems

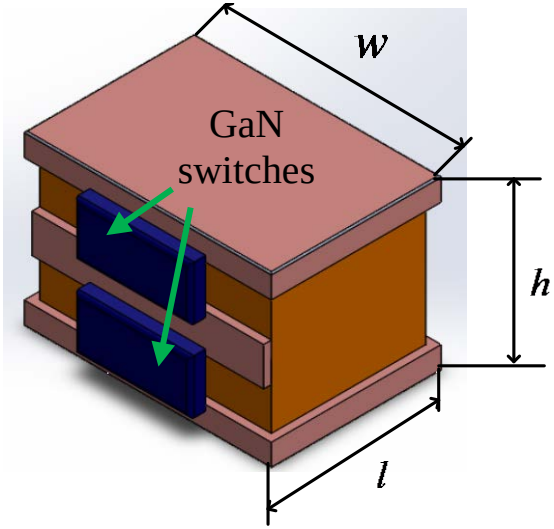


	Turn-on / (Turn-off)
L_{int1} [nH]	0.27/0.26
L_{int2} [nH]	0.23/0.17
L_{int3} [nH]	0.24/0.43
L_s [nH]	0.57/0.89
L_d [nH]	1.89/1.62

Liu, Z et al. IEEE PELS Transactions 2014

Parasitic inductance of capacitor

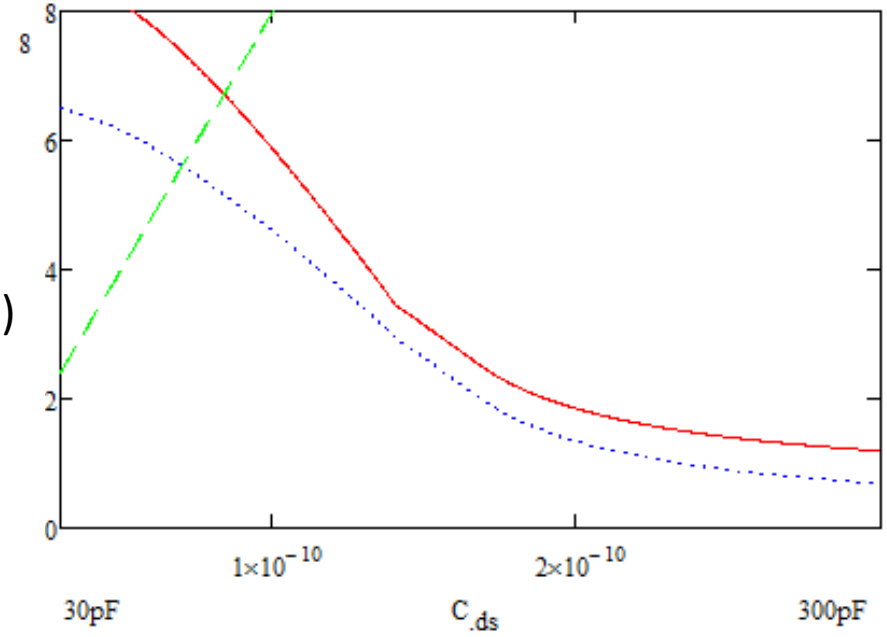
- ZVS, zero turn-on loss
- Turn-off loss become limit
- Even with zero layout inductance, parasitic inductance of capacitor increases the turn-off losses



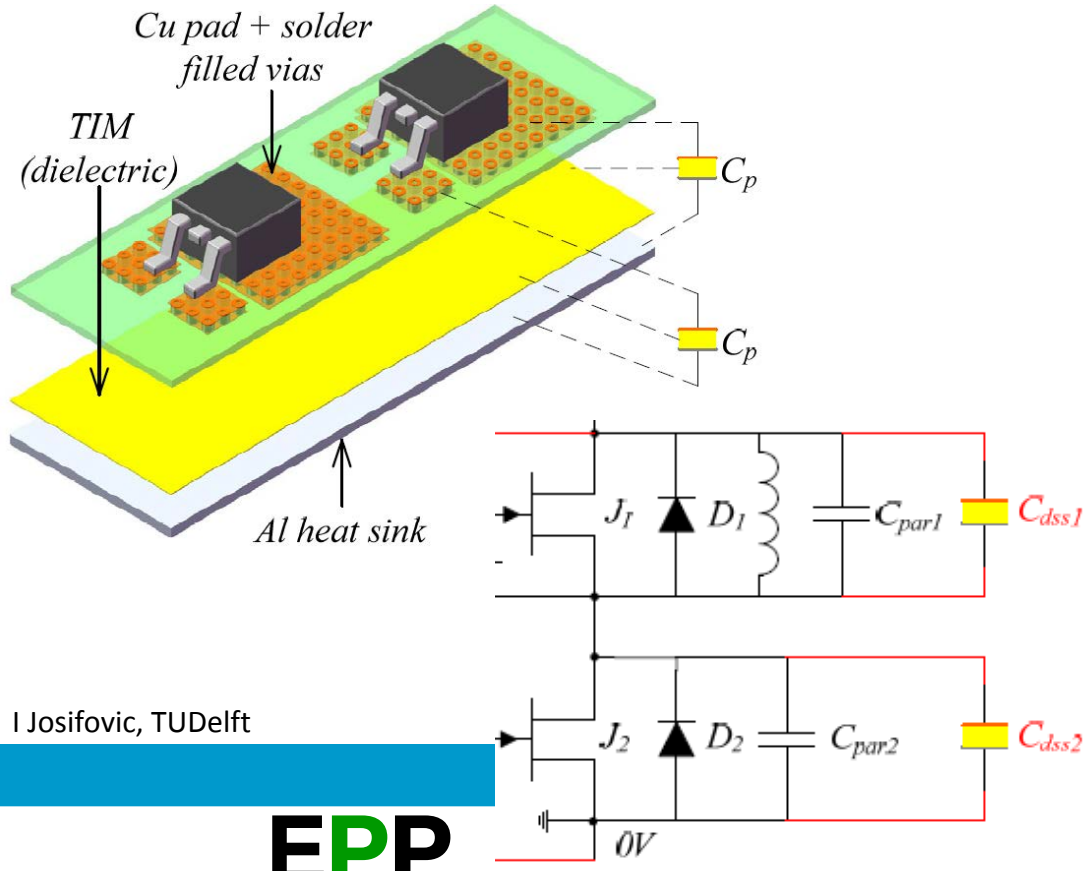
$P_{turn\_off}(C_{ds,}5nH)$

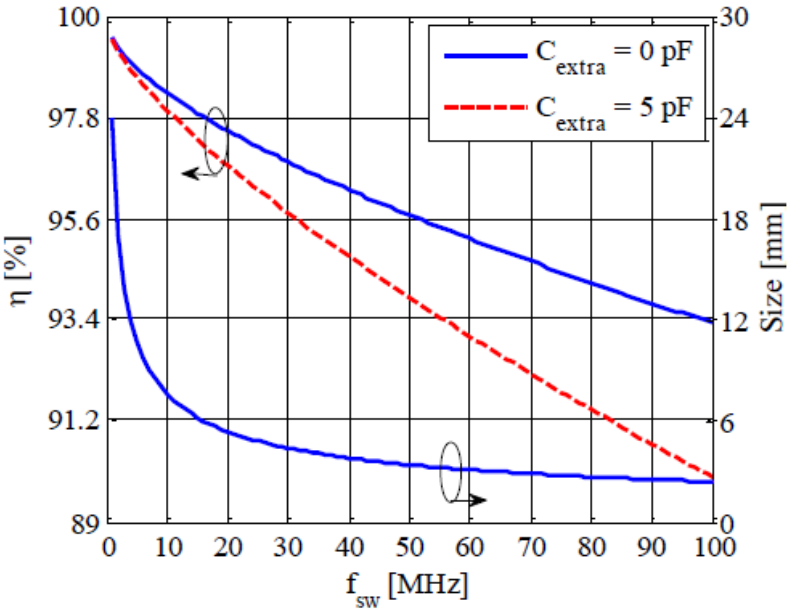
$P_{turn\_off}(C_{ds,}0.5nH)$

$P_{turn\_on}(C_{ds})$



- Not only inductances but parasitic capacitances
  - Parasitic capacitive coupling through thermally enhanced PCB
  - 25% total loss increase in SiC inverter (~16kHz, 100pF par vs 60pF device)
  - VHF GaN-on-SiC - 5pF of additional parasitic capacitance @40MHz results in 50% loss increase





I Josifovic, TUDelft

Maksimovic, ECCE2013

EPP

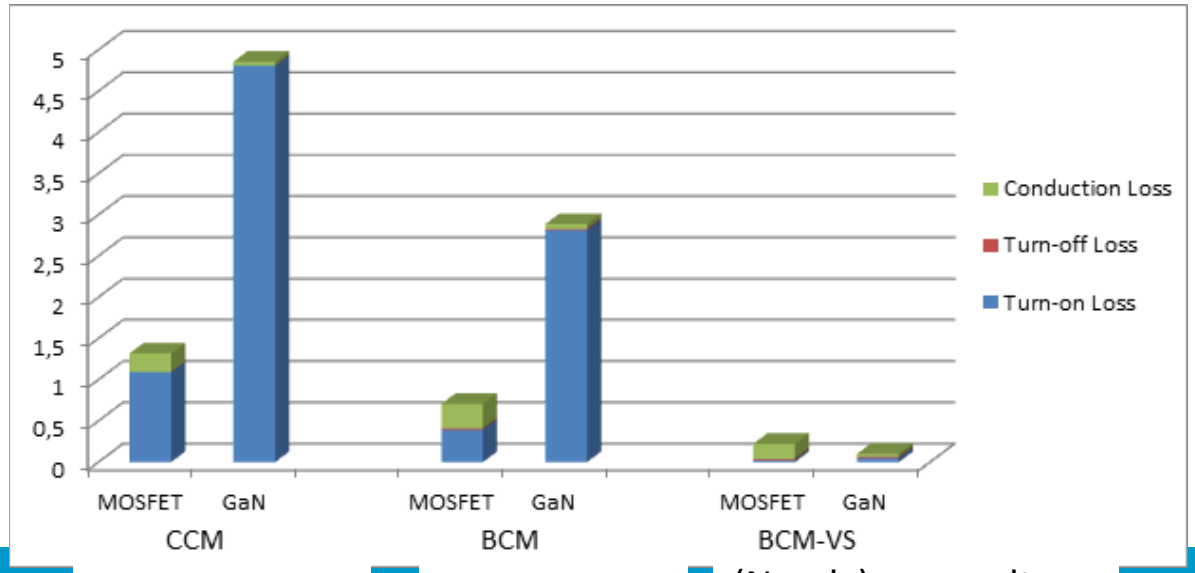
Electrical Power Processing

TU Delft

- Topologies and operation modes “immune” to or utilising package and circuit parasitics (ZVS, valley-switching, resonant pole inverter)

- 3D integration approaches for reducing parasitics, but often at the cost of thermal management

P_{loss}[W]



100W, 1MHz, boost

W. Wang, TUDelft

Hard switching

Zero-current swtiching

(Nearly) zero-voltage switching

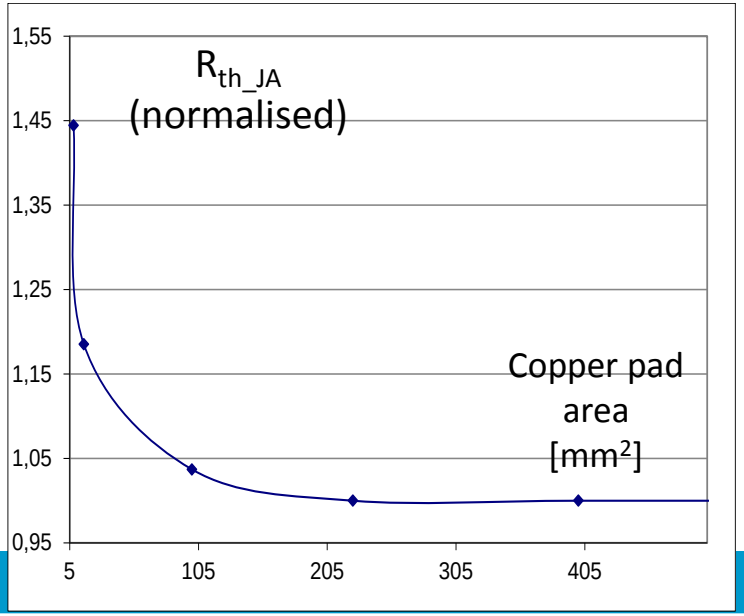
Thermal management

- Challenges from the die to system level

- TO-220 the thermal resistance junction-to-case (R_{th_JC}) for the GaN device is double that of a super-junction MOSFET with the same R_{dson} (1.55K/W vs. 0.8K/W)
- Flip chip devices – solder bumps dominant in junction-to-board (R_{th_JB}) thermal resistance (15-35K/W)
  - Cu solder bumps reduces it but still 2X higher than backside mounted die

Limitations of PCB heatspreading

- Due to the very small die surface area, the effectiveness of heat spreading on a standard PCB stack-up is limited.
- For a small die, even the thermal resistance of an “infinite” heat spreader is prohibitively high.
- Thermal vias and bottom heat spreader – thermal resistance junction-to-ambient R_{th_JA}=27K/W (100vias/cm^2) compared to 77K/W. Still dominated by junction-to-board thermal resistance (R_{th_JB})



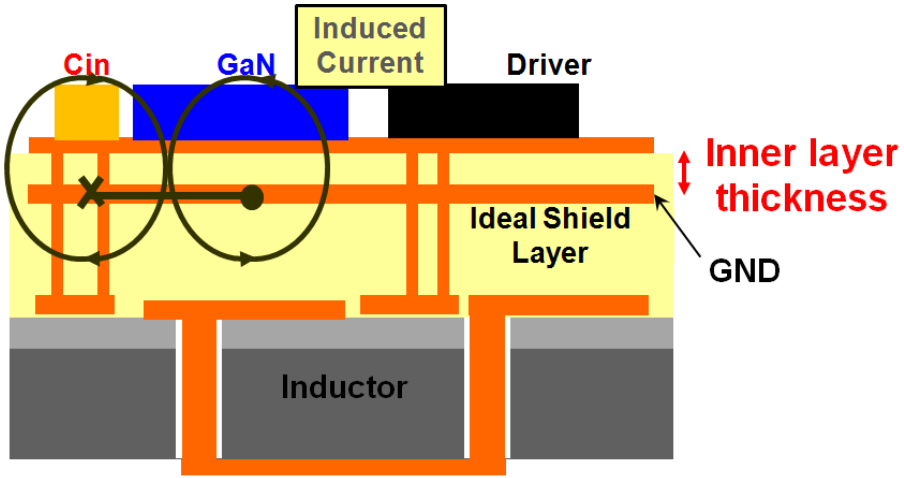
Thermal vias (100vias/cm^2), 1mm spreader, 70µm Cu
*(thicker Cu not recommended since it is practically impossible to make reliable pads for the components).

- Thermal vias and heat spreader cause capacitive coupling to the heat spreader
  - ~50pF for TO-220 package, compared to 25pF-50pF of the device
  - For flip-chip packages, thermal spreading should be done on drain contact of top and source of the bottom device to minimise equivalent parasitic capacitance

- Reflow soldering and thermally enhanced substrates – cost prohibitive in some applications (consumer applications need heat sink/wave soldered packages)

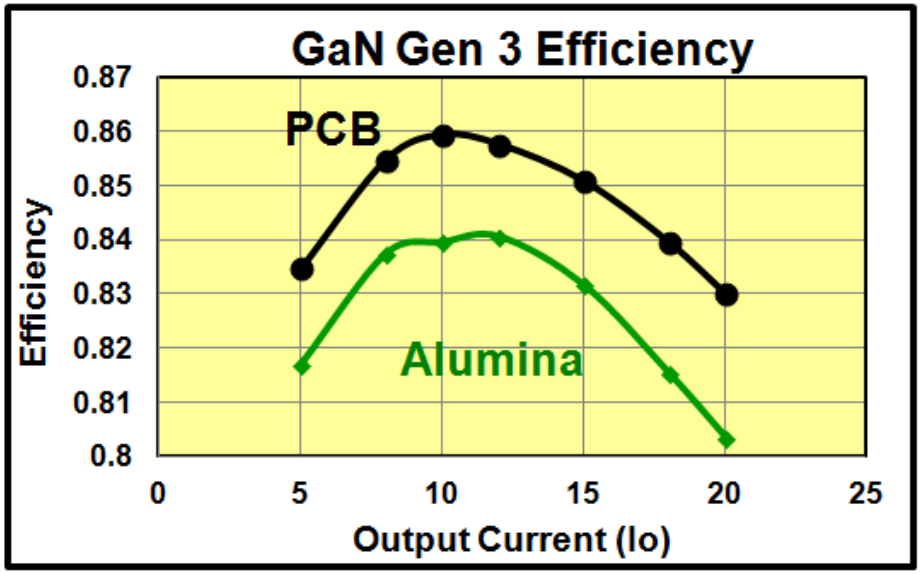
Higher thermal conductivity circuit carriers

- Instead of PCB
  - DBC vs PCB – lower thermal resistance <u>but</u> higher losses due to larger parasitic inductance due to distance of the Cu layers
  - IMS – lower thermal resistance <u>but</u> parasitic capacitive coupling due to thin dielectric, single layer routing



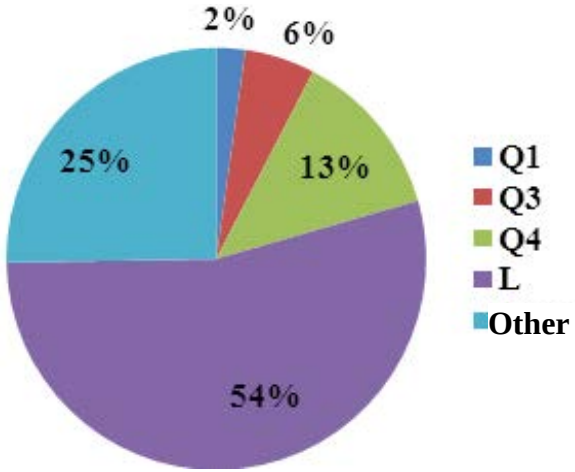
D. Reusch, PhD thesis, Virginia Tech

0.38mm DBC



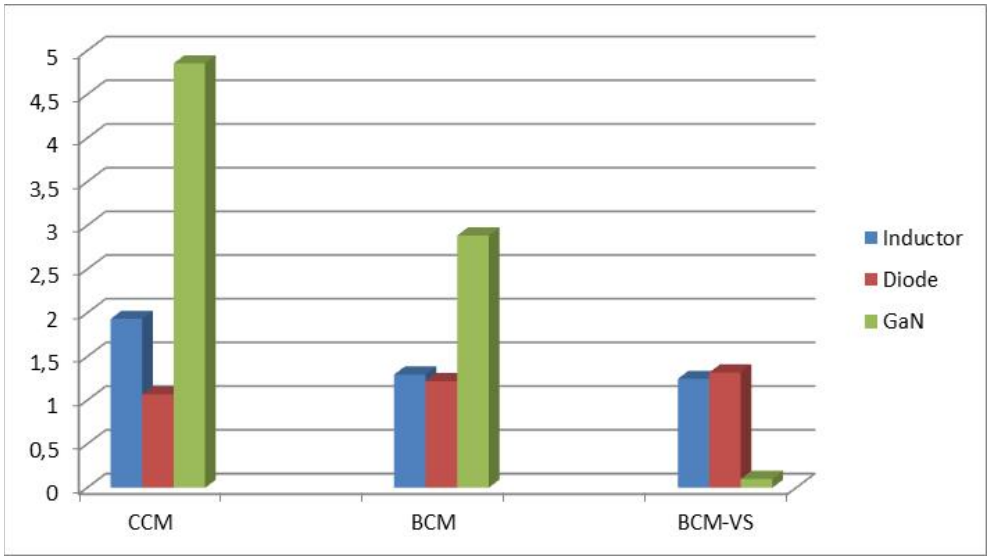
Large portion of losses in passive components

- Shift in loss distribution between semiconductors and passives*
  - Pushing switching frequency up limited by passives (magnetics)



Thin-film PV panel integrated DC/DC converter, 100W, 1MHz

Acanski, TUDelft

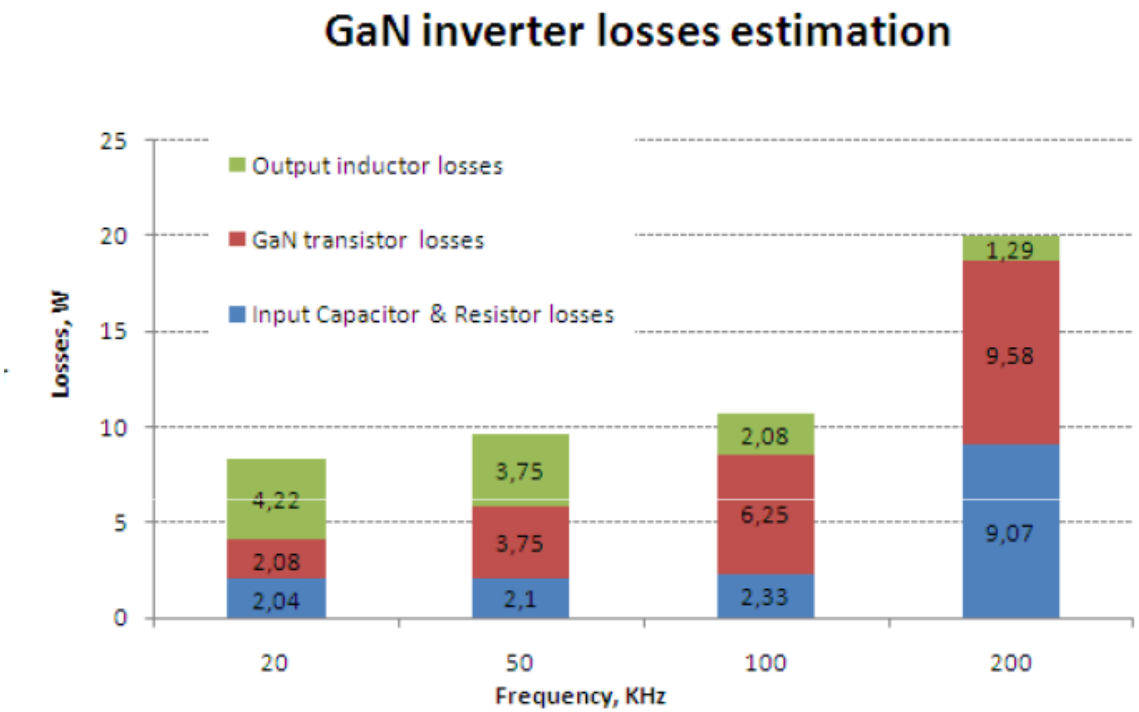


Boost PFC 100W, 1MHz

Wang, TUDelft

Large portion of losses in passive components

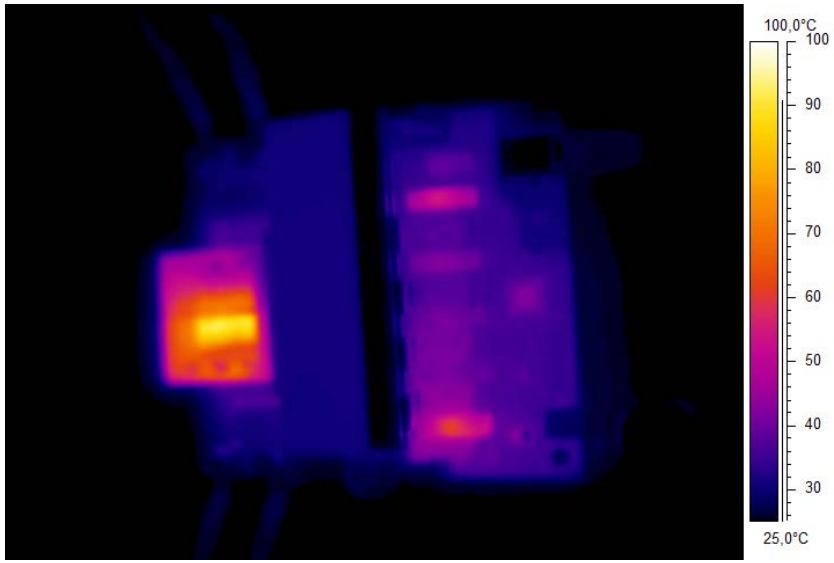
- The losses in the DC capacitors increase highly with the GaN devices because of hf currents in the DC bus (inverter, 200W, 200kHz)



Mitova, Schneider Electric r, ECPE seminar 2013

- Cooling of passives becomes limiting factor

Kranzer, Fraunhofer, ECPE seminar 2013



Transformer @90°C
Transistors @30°C

Josifovic, TUDelft

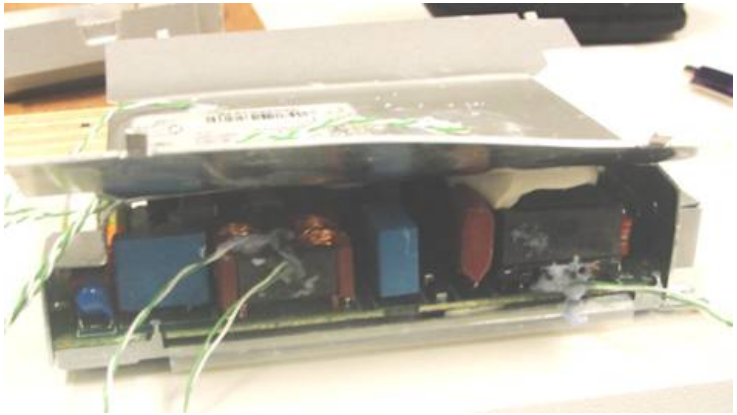
SiC JFETs @83°C
Elec. caps @70°C

High packaging density, thermally enhanced elcaps

Cooling of passives – alternative approaches

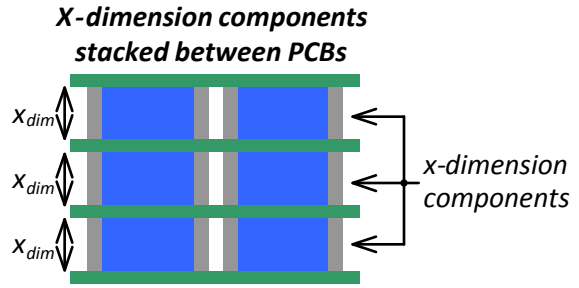
- 3D heat spreading concepts and materials
- Overmoulding of passives with thermally conductive materials
- Enhancing passives with thermally active materials
- Multifunctional use of converter parts electrical/ thermal/ mechanical

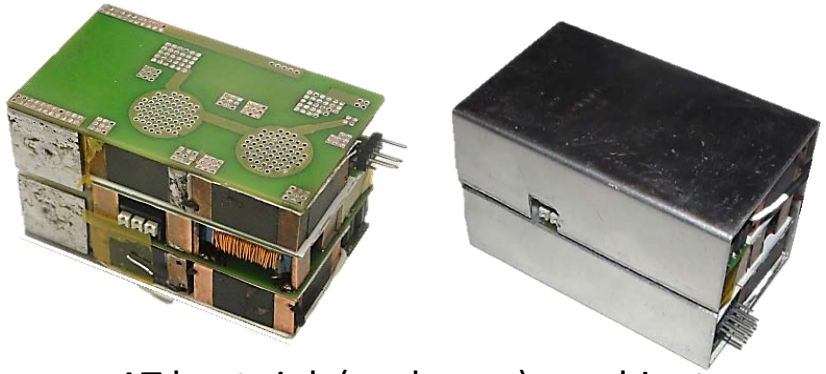
- Thinking on system level instead of Rth_{j_c}
  - Lower temperature drop throughout converter, smaller heat sink
  - Modular based architectures – better heat distribution
  - Power sandwich example (HID)



ΔT heat sink (enclosure) - ambient:
$\Delta T_{a\text{-}hs}$=26°C (average)

2X size reduction



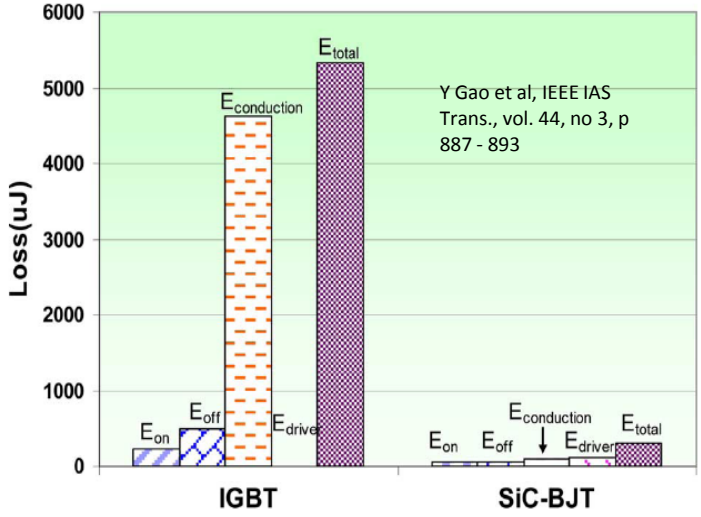


ΔT heat sink (enclosure) - ambient:
$\Delta T_{a\text{-}hs}$=45°C (average)

Reduce ΔT in components to allow larger ΔT from ambient to case (heat sinks) →
→ Smaller heat exchange elements!

What if we had materials with 10x better active materials?

- Semiconductors: SiC and GaN devices
- Dielectrics: nano materials and ceramics
- Magnetics: nano materials and new high permeability compounds



Dielectrics

Energy Storage Density

Dielectric Material	E_{max} [V/µm]	ε_r	$W_{vol,max}$ [J/cm³]	$W_{vol,typ}$ [J/cm³]	@ nominal device voltage
Polypropylene (BOPP)	450	2.2	2.0	0.1 … 0.125	500 V
Polyester (PET)	280	3.2	1.1	0.025	100 V
Polyphenylenesulfid (PPS)	320	3.0	1.4		
$BaTiO_3$ based ceramics	10 (60)	2500 [1)]	0.5…1 [2)]	0.1…0.175	500 V
Optimized ceramics [3)]	60…90	350	4…6		
SiO_2	1200	3.8	24		
Al_2O_3	800	9	25		

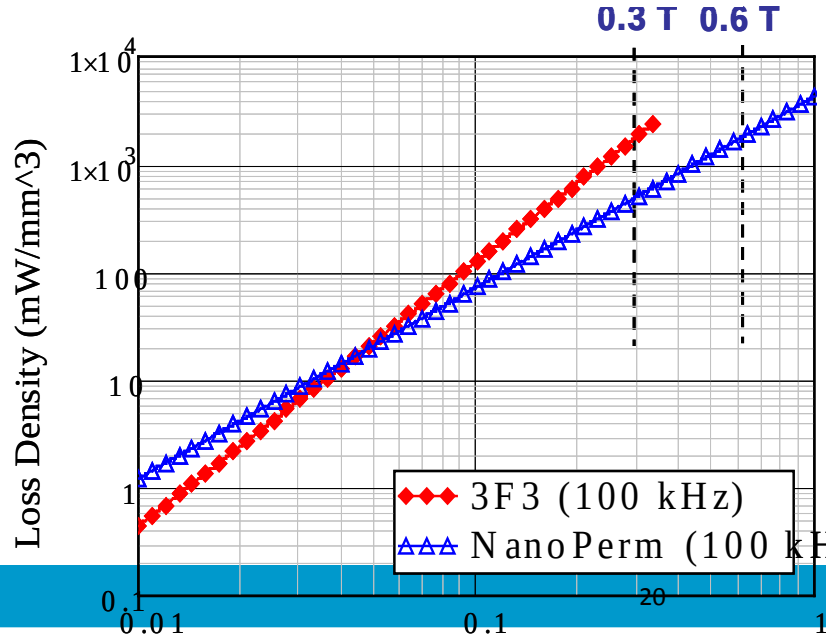
Material limits [4)]

Energy density of available capacitor devices

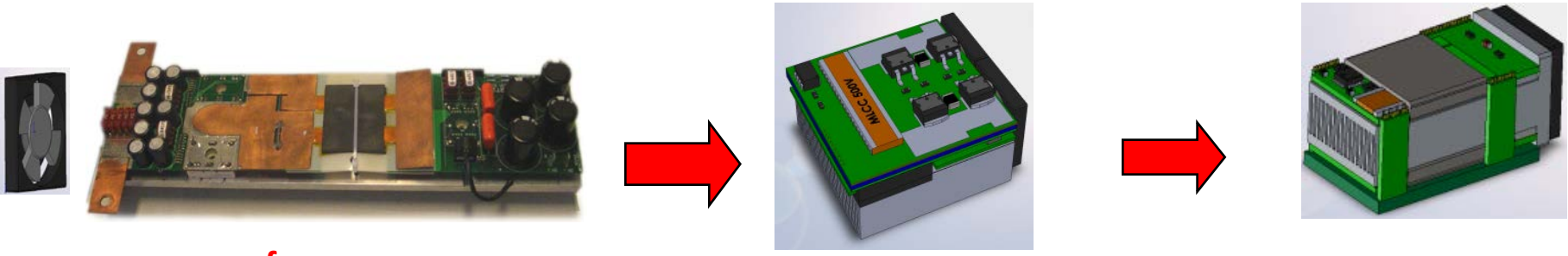
Max. Storable Energy

$$W_{vol,\,max} = \frac{\varepsilon_0\,\varepsilon_r}{2}\,E_{max}^2$$

M. Maertz, Frauenhofer, ECPE passive component seminar, 2007



- Volume of electrically active parts decreases – relative volume of thermal management parts can increase

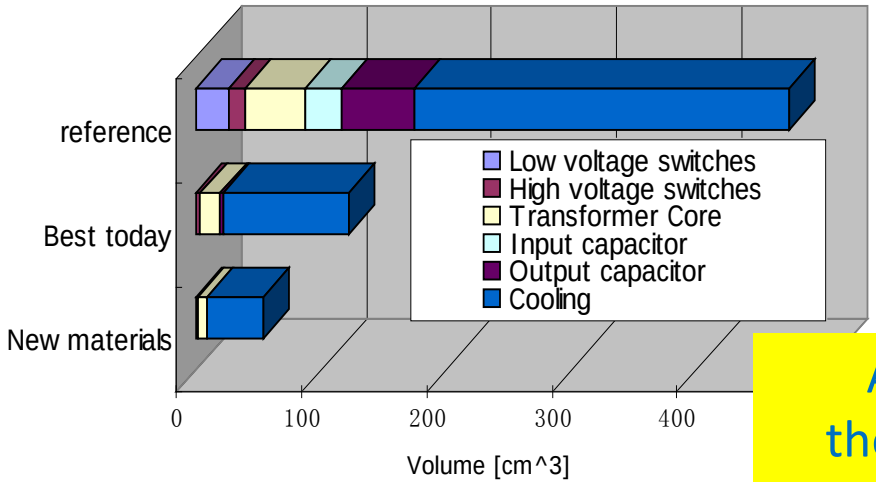


reference

Best today

New materials

Volume breakdown



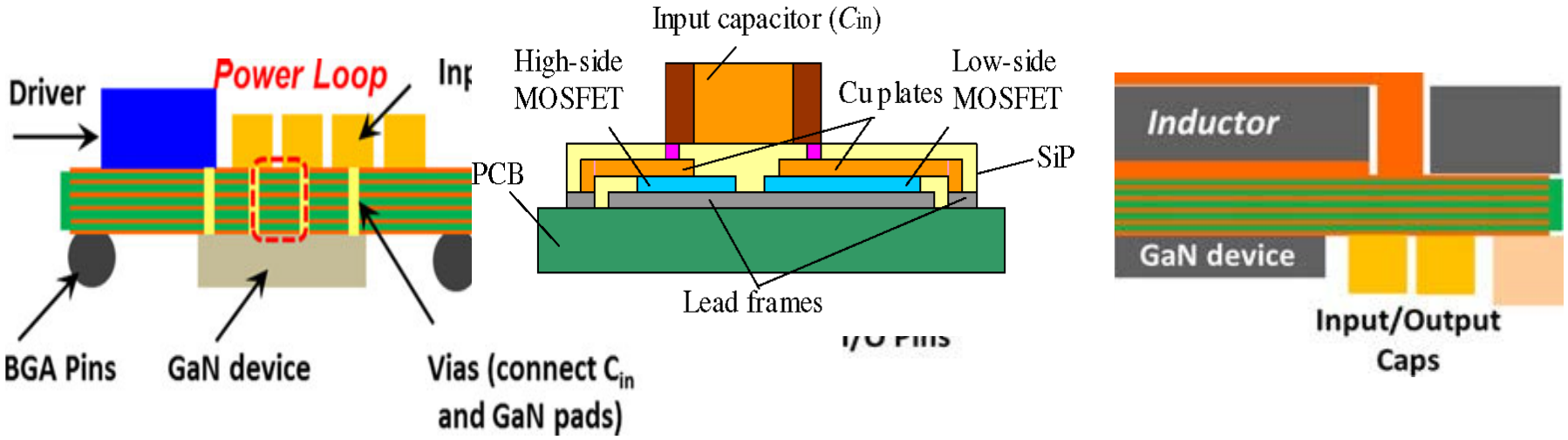
Comparison 12V – 400V isolated dc/dc converter

Y. Wang, TUDelft

After functional and packaging integration, thermal management becomes the bottleneck

3D System Integration

- Technology platform for 3D placement of switching and electromagnetic function and optimal heat distribution
  - Trade-offs switching performance/heat removal/integration
- Commutation cell basic building block



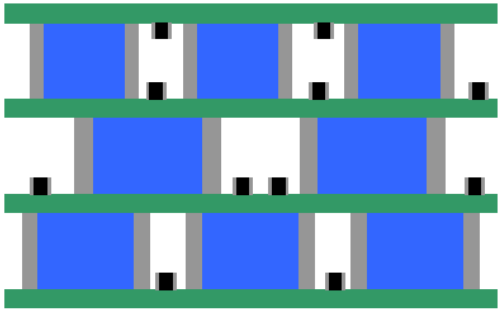
Shu Ji et al."High-Frequency High Power Density 3-D Integrated GaN Point of Load Module Design," IEEE Transactions on Power Electronics, Sept. 2013

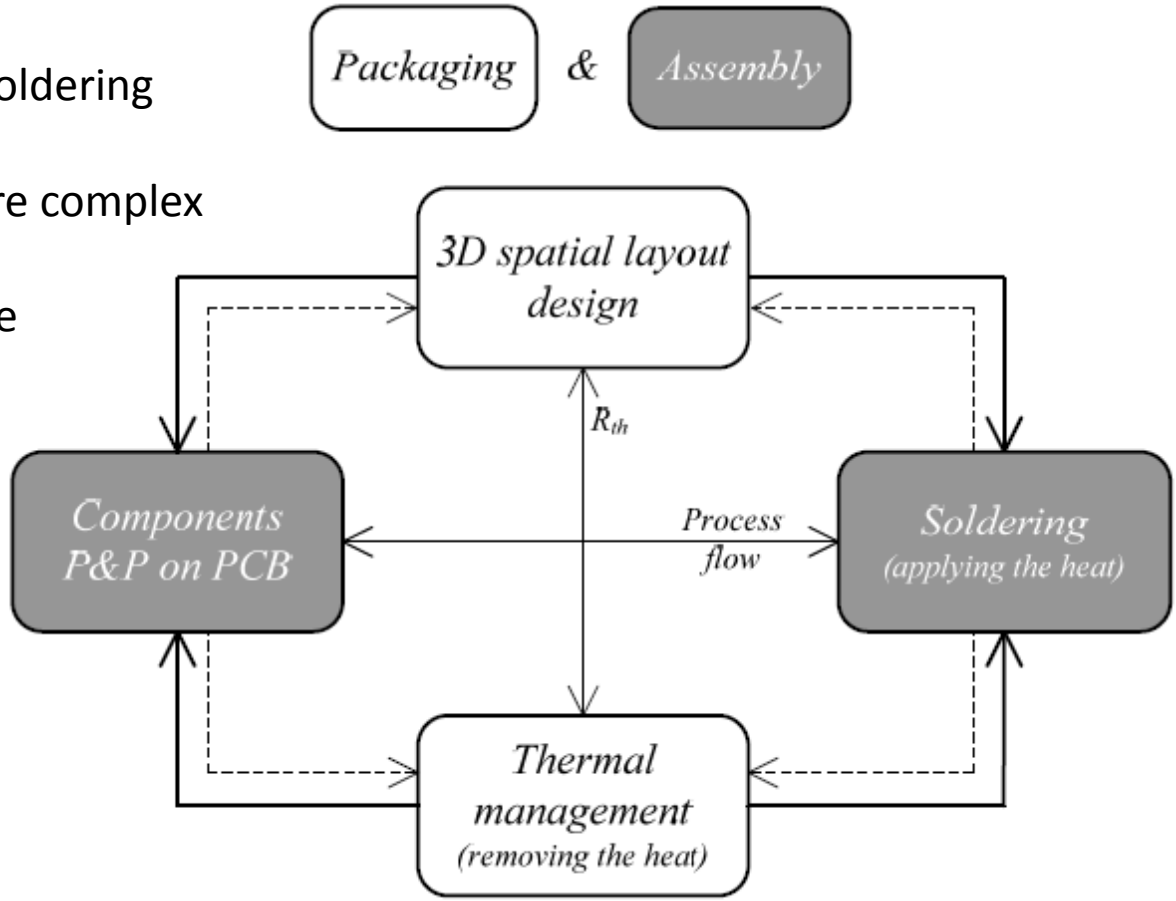
Hashimoto, T. et al.,"A System-in-Package (SiP) With Mounted Input Capacitors for Reduced Parasitic Inductances in a Voltage Regulator," IEEE Trans on Power Electronics, March 2010

- Suitable for automated manufacturing (Power Sandwich example)
  - Thermal management/assembly trade-offs

- Better thermal management vs. soldering temperature profile
- 3D high density packaging vs. more complex soldering process
- SMT assembly line vs. P&P of large components

Power Sandwich assembly





Power density

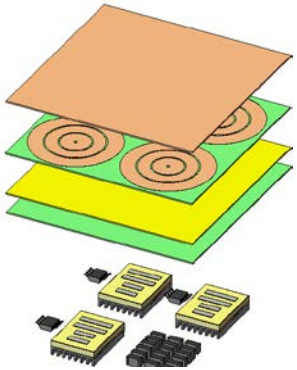
50kW/dm³

20kW/dm³

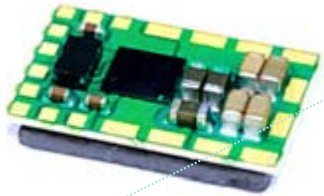
5kW/dm³

500W/dm³

VHF GaN
PCB
embedded



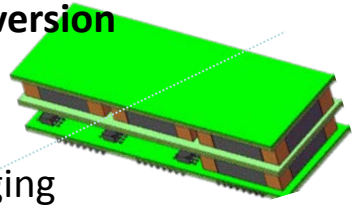
GaN MHz POL
LTCC ind



Si MHz POL
SiP

Low voltages

MHz line voltage conversion (GaN)
SMT passives
Multilayer PCB packaging



Line voltages

Si conversion
2D layout

Switching frequency

80kHz

1MHz

5MHz

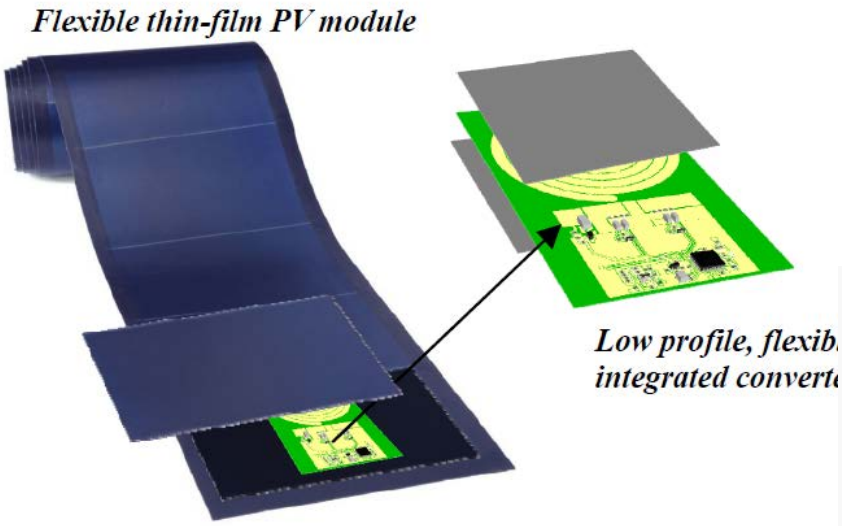
30MHz

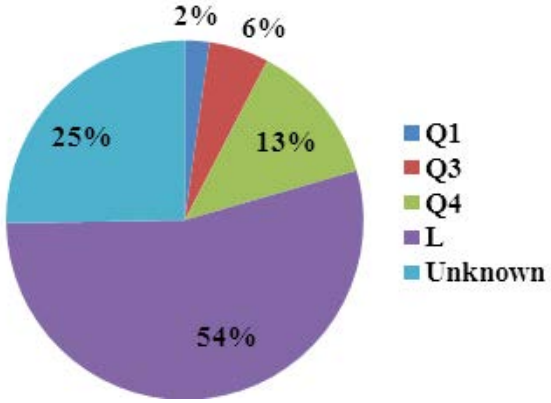
EPP
Electrical Power Processing

TU Delft

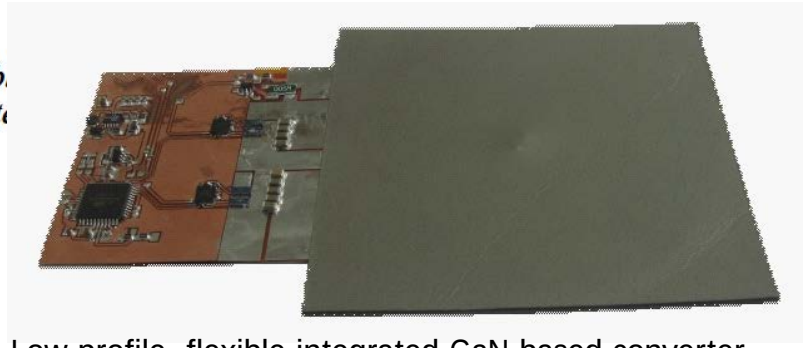
Technology platforms and applications

- PV module integrated converter
  - High efficiency, low profile, flexible
  - Lossy inductor, thermal management





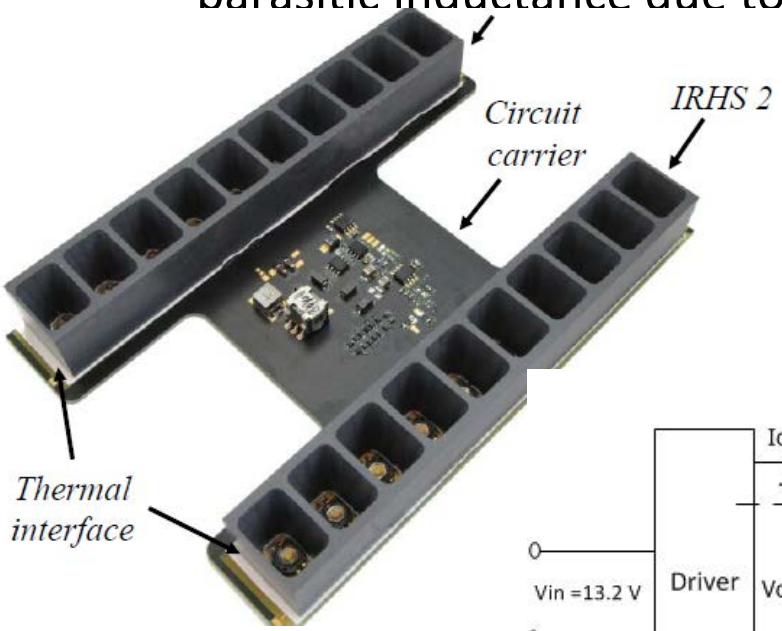
Loss distribution



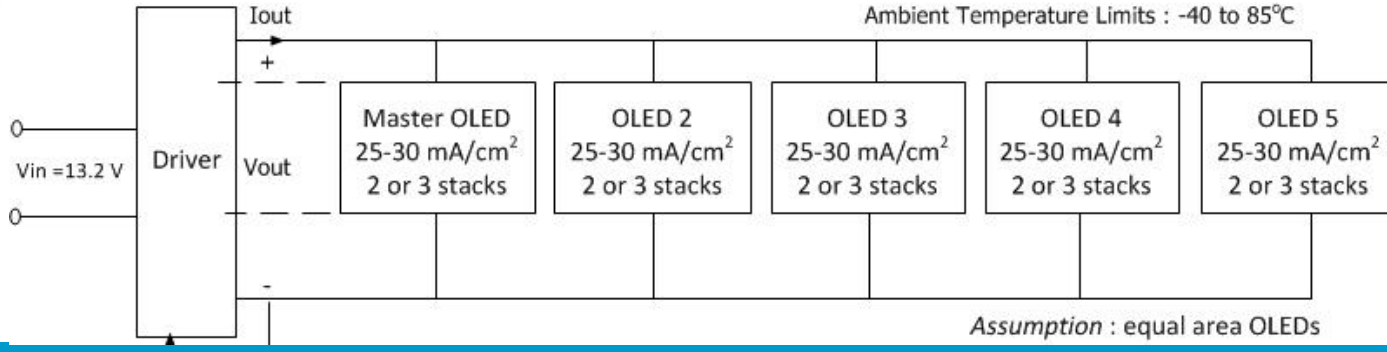
Low profile, flexible integrated GaN based converter

M. Acanski, TUDelft

- Automotive LED(OLED)
  - 3D MID technology platform for 2.5D integration of mechanical/optical functions
  - Thermal management a challenge (thin Cu: 10-15µm, no multilayers), parasitic inductance due to limited routing options

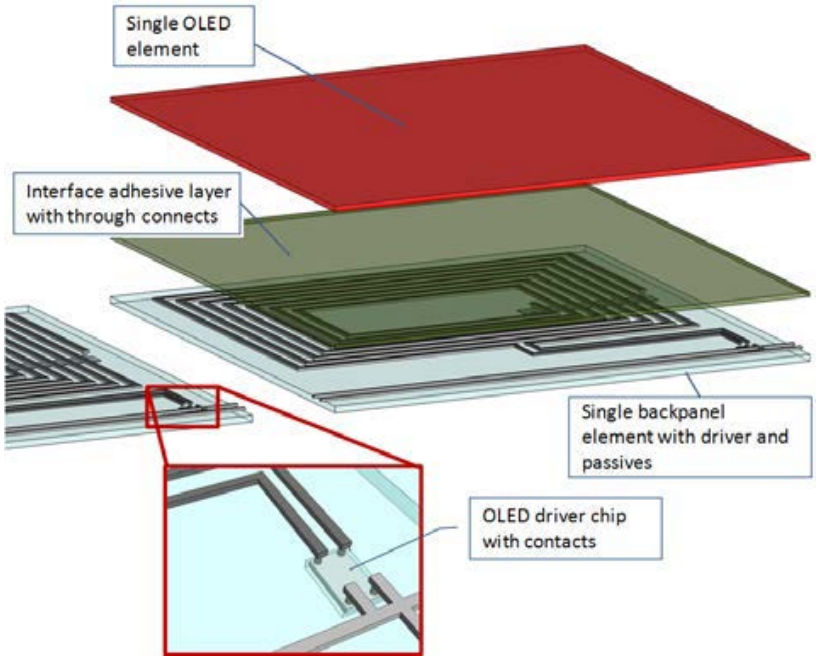


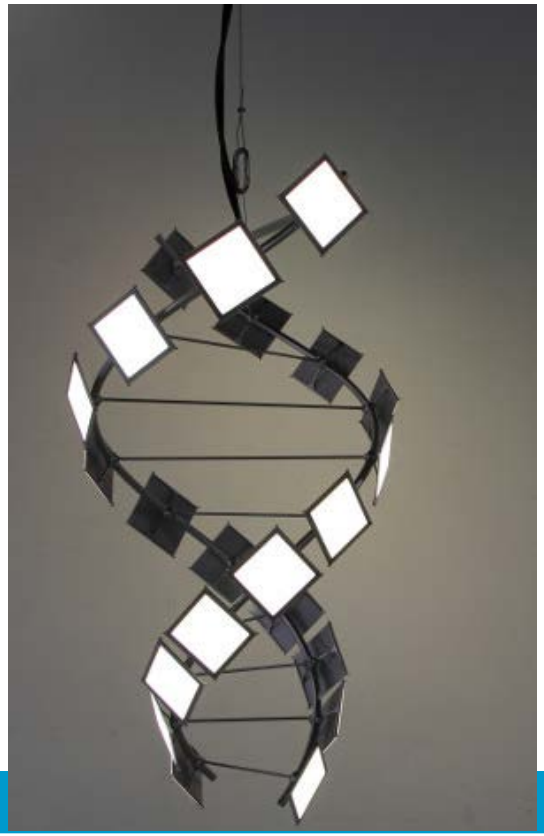
Driving 5 OLEDs



W. Thomas, Ingolstadt & TUDelft

- OLED lighting designs, converter per panel for individual control
  - (Very) low profile, high efficiency, flexible
  - Large series resistance and parasitic capacitive coupling between the coil and cathode
  - Si solution, 10MHz, 71% efficiency

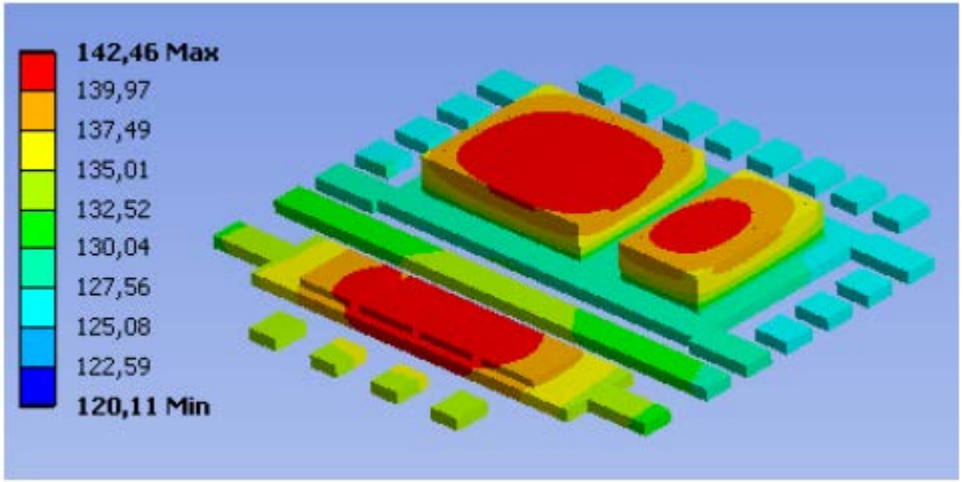


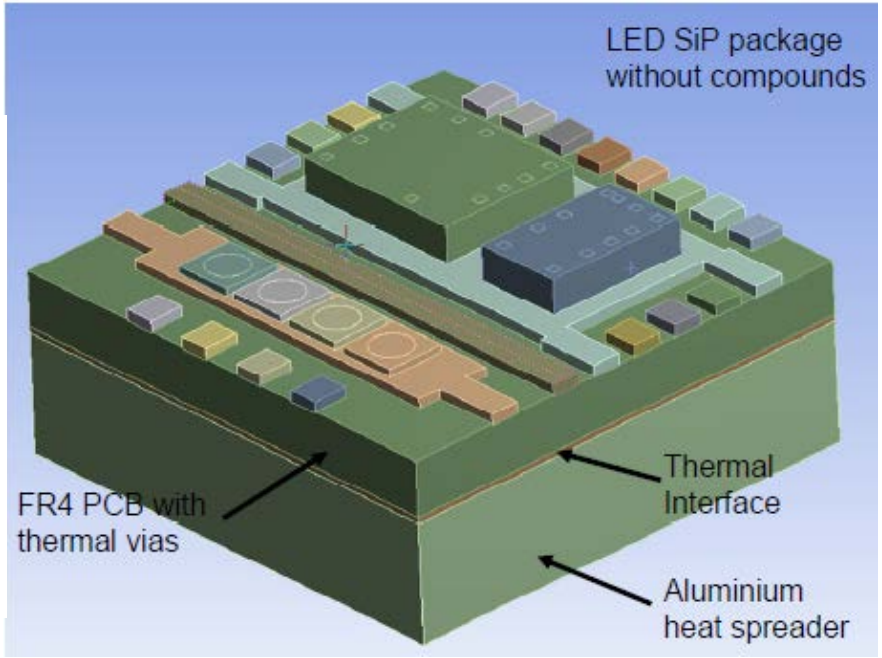


Si solution, 10 MHz, 40V-7V@350mA, 71% efficiency

"J. Doutreloigne et al. "Design of an Integrated OLED Driver for a Modular Large-Area Lighting System", CSS2013.

- SiP LED (OLED) driver – driver and lighting function
  - Too high temperature rise
  - Reducing losses with GaN





"Development of an intelligent integrated LED system-in-package" Gielen et.al.

Final remarks

- Many new possibilities (and technology evolution steps) enabled by GaN devices but surplus of challenges too.
- Proper handling and exploitation of parasitics (inductive and capacitive) is crucial for exploiting full potential of GaN devices.
- New converter packaging technologies, spatial layouts and thermal management approaches needed
- Better large volume production and assembly technologies are needed for important application pulls